AN ANALOG-DIGITAL CMOS SEMICUSTOM ARRAY FOR HIGH-PERFORMANCE MIXED-MODE ASICs

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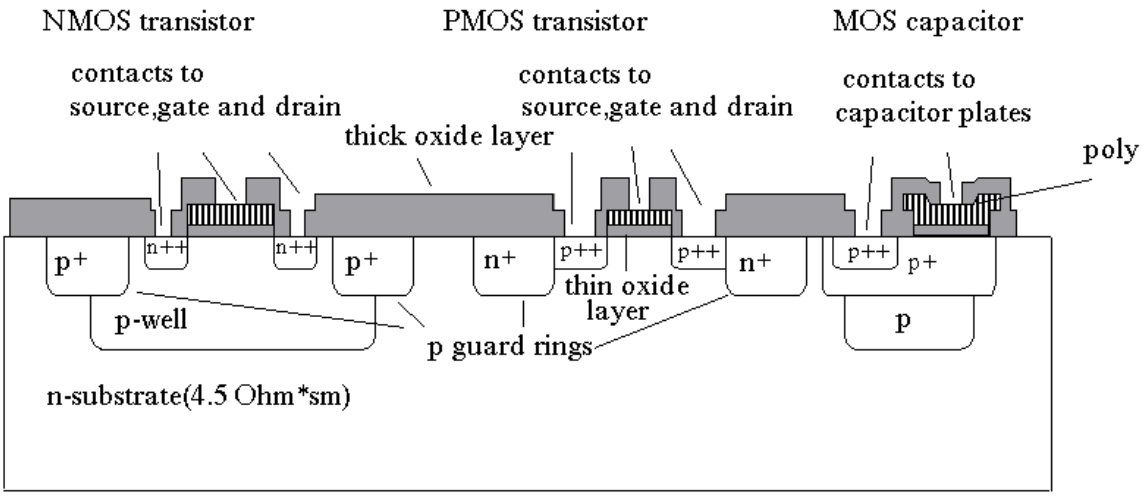
Abstract. **A standard-digital-CMOS-process-compatible analog-digital CMOS semicustom array architecture is presented. The array is suitable for high-performance SC circuit design, though, other circuit techniques such as SI and continuous-time analog signal processing are possible. Main cells of an analog standard cells library are presented as well as experimental results of testing some SC systems such as the 5-th order elliptic SC low-pass filter and the 10-bit DAC are discussed.**

1. Introduction

One way to reduce an ASIC design schedule and cost is the use of the gate array design methodology. Whereas the swithed current (SI) circuit technique becomes increasingly popular in analog-digital mixed-mode ASIC design during last years, the SC circuit technique still, nevertheless, demonstrates significantly better state-of-the-art performance in terms of circuit accuracy characteristics (dynamic range, sample-to-sample circuit parameter deviations, etc.) in comparison with the SI one. Unfortunately, the SC technique requires from the process the availability of precision capacitors, so to adopt SC techique for ASIC array-based design within a standard digital CMOS process is not an obvious task. One way to meet the requirement involved is the use of analog-digital semicustom arrays having separate basic structures for the analog and the digital parts. In this paper we present such type of array architecture and some examples of SC design based on that array. The array architecture makes it possible to use precision voltage-independent thin-oxide MOS capacitors and the array is, nevertheless, fully compatible with the standard digital 5 V 3-micron CMOS process.

2. Analog-digital array architecture

The architecture of the array considered differs from conventional digital CMOS gate arrays by the availability of a dedicated analog field containing specific analog devices such as array of analog long-channel floating-well MOS transistors, MOS capasitors, poly resistors, CMOS switches of minimum size (optimal for SC circuits), p-n junction array for built-in bandgap voltage reference and absolute temperature sensor. The main specific analog requirement supported by this field is the availability of a high-quality thin oxide MOS capacitors array. Fig.1 shows a cross-section of a standard self-aligned two-metal-and-one-poly CMOS digital process being used for the array basic layers implementation as well as the MOS capacitor implementation within the process considered: as one can see the capacitor is realised using a p-guard ring diffusion region as the capacitor's bottom plate, poly gate layer as the capacitor's top plate and thin oxide layer as the capacitor's dielectric. Though the p-guard ring region is not the highest doping concentration region of the process, its doping concentration is, nevertheless, high enough to overcome any appreciable voltage dependance of the capacitance value. The stucture has a significant bottom-plate parasitic capacitance (up to 50% of its nominal value) but this drawback can be made negligible by correct circuit design. Three 1-pF-unit capacitors (and several small non-unit capacitors for capacitance fine adjustment), two 10 kOhm-unit resistor and two minimum-size CMOS switches form a single array cell and 84 cells form an array, so-called SRC-array.



. Fig.1

The entire array architecture is shown in Fig. 2 as well as an array-based test chip layout.

The field of active analog cells is an array of analog long-channel MOS transistors (including transistors with separate wells for differential pairs realisation). It is possible to realise up to 36 two-cascade op amps within this field.

The field of output buffer analog cells consists of MOS transistors having different W/L ratios optimized for the class-AB-output-stage op amp implementation. It is possible to realise up to 6 such op amps as well as a built-in bandgap voltage reference within the field considered.

The field of logic gates consists of about 1500 non-connected CMOS logic gates.

To prevent digital circuit operation influence upon the analog part, separate power and ground buses/pads for the analog and the digital parts are provided.

The architecture involved is intended basically for SC design (SC filters, SC ADCs and DACs, SC signal processing systems, etc.) but the availability of resistors and long-channel MOS transistors makes it possible to design continuous-time systems consisting of op amps, resistors, capacitors, MOS resistive circuits /1/ and current mirrors, for example, continuous-time MOS filters, parallel flash ADC, current-steering DAC, voltage multipliers, etc. Of course, the switched current design is possible also and in this case both analog or digital fields of the array could be used.

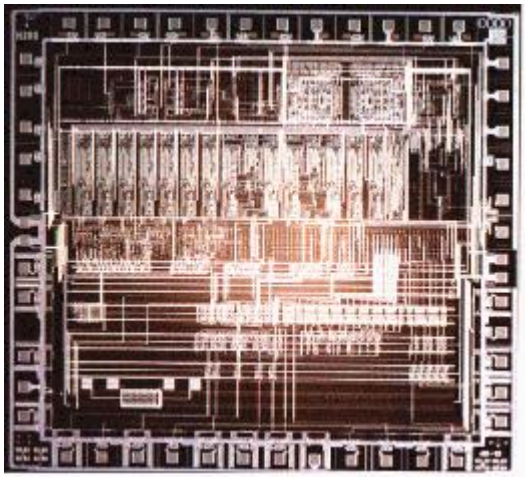


Fig. 2

3. Analog cell library

The analog cell library of the array considered consists of a two-stage cascode op amp with a class-A output stage, op amp with auxiliary inputs for offset voltage compensation, op amp with a class AB output stage, comparators, Shmitt trigger, MOS resistive circuit, four quadrant analog multiplier, binarily-weighted capacitor array, uniform capacitor array, second-order SC filter sections, bandgap voltage reference, bias circuits, etc.

The most frequently used cell is the two-stage cascode op amp with a class-A output stage. This op amp is intended to be used for SC systems (primarily, SC filters) design. There are many types of CMOS op amps being used in SC circuits: OTA, cascode OTA, two-stage op amp configuration, the cascode one, high-gain invertors, etc.; and there is no an unequivocal answer to the following question: which configuration is better for SC applications. The popular cascode OTA is a good decision due to its simplicity, low power consumption and good stability without frequency compensation circuit (capacitive load in SC circuits ensures sufficient phase margin in this case) but some drawbacks of this structure can restrict its application. For example, the unsufficient voltage gain does not allow to reach the necessary Q-factor value in high-Q-factor filters and the necessary resolution in precision A/D and D/A converters, limited output voltage swing can become a serious problem in modern submicron processes with low power supply voltage. Moreover, very high output impedance of cascode OTA can cause input-to-output interaction in serial SC stages because the cascode OTA output can not be considered as a voltage source. That is why we have chosen the two-stage cascode op amp configuration. The simplified circuit diagram of this op amp is shown in Fig. 3. The complete op amp circuit differs from Fig. 3 by presence of minimal-size transistors ensuring that there is no current consumtion when the ENABLE control input (not shown in Fig. 3) is high (power-off sleep-mode). This opportunity is very important for chip testing. Note that the input transistors MN2, MN3 are implemented in their own well that reduces noise.

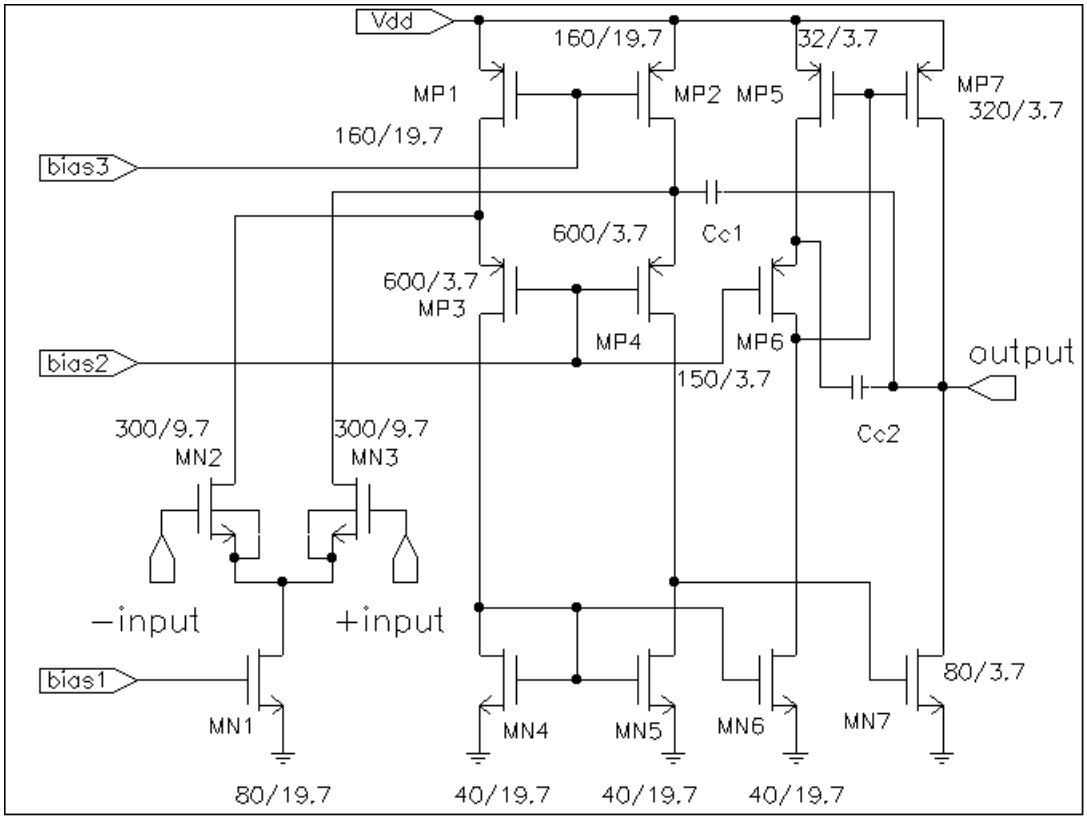


Fig. 3

A two-stage configuration means that the op amp design becomes more complicated, first of all, due to a necessity of frequency compensation. A problem is that the simplest Miller compensation causes a significant reduction of power supply rejection ratio at high frequences that results in significant degradation of SC circuit performance. We have realised the cascode compensation using Cc1 and Cc2 capacitors in such manner that there is no AC signal path from power supplies to the op amp output (except for that through the transistors' own parasitic capacitances) due to the fact that left plates of Cc1 and Cc2 capacitors are at the virtual ground potential, thus, the power supply rejection ratio does not degrade significantly at high frequencies. Experimental measurements of the op amp show that it has the following performance characteristics (at 5 V power supply):

- voltage gain is 86 dB;
- input offset voltage does not exceed 5 mV (most of op amp samples have less than 1mV offset voltage);
- supply current is about 70 uA (its value can be programmed in a wide range);
- unity gain bandwidth at 20 pF load is about 2 MHz.

On the basis of the op amp considered the op amp with auxiliary inputs was developed. It was achieved by means of parallel connection of the main differential stage with an auxiliary differential stage having very low transconductance in comparison with the main one. Input offset voltage compensation (autozeroing) and double-correlated sampling for low-frequency noise reduction can be easily performed by means of the auxiliary inputs for high-performance applications. We have used this op amp in 10-bit DAC.

The two-stage cascode op amp with a class-AB output stage is necessary for such application as output buffering of analog signals in voltage follower configuration, operation with low impedance load, operation with resistive feedback (formed by MOS resistive cells or poly resistors), etc. For the applications considered it is necessary to ensure the op amp maximum output current value that is many times of its output stage bias current. A simplified circuit diagram of the op amp is shown in Fig. 4 /2/. The complete op amp also contains turning-off transistors for testing. The op amp considered differs from the Fisher and Koch structure /3/ by introducing the first stage common-mode output voltage feedback loop. Let us note that the NMOS differential pair (MN2, MN3) is in the cut-off state if the input common-mode voltage is close to the negative power supply and the PMOS differential pair (MP2, MP3) is in the cut-off state when the input common-mode voltage is close to the positive power supply, thus, the first stage bias current varies significantly over rail-to-rail input common-mode voltage range. The feedback loop involved is implemented by means of the common-mode voltage amplifier (transistors MN14, MP14-19. This allows to stabilize the operating-point voltage of the first stage at the analog ground potential over rail-to-rail common-mode input voltage range independently of process parameters spreads and supress voltage spikes penetrating from power supply buses, thus, this configuration would be suitable for analog-digital mixed-mode application. The frequency compensation circuit of the op amp considered is quite complex and not shown in in Fig. 4. The experimental measurements of the op amp give the following results at 5 V power supply voltage :

- voltage gain - 92 dB;
- input offset voltage - does not exceed 5mV;
- supply current (could be programmed in 20 uA - 5 mA range) - 500 uA;

- unity gain bandwidth (at 20 pF load) - 3 MHz, op amp stable for any load capacitance value;
- input voltage common-mode range - rail-to-rail;
- output voltage swing at 500 Ohm load - rail-to-rail ex 0.8 V value.

The op amp can drive a 220-Ohm earphone with +/- 2 V output swing (in 0.3-5 kHz frequency range).

The class-AB op amp in conjunction with two MOS resisitive cells forms a four-quadrant analog multiplier. Measurements show that it has satisfactory linearity (non-linear distortions do not exceed 2-3 %) at +/- 0.5 V input voltage range for both X and Y inputs.

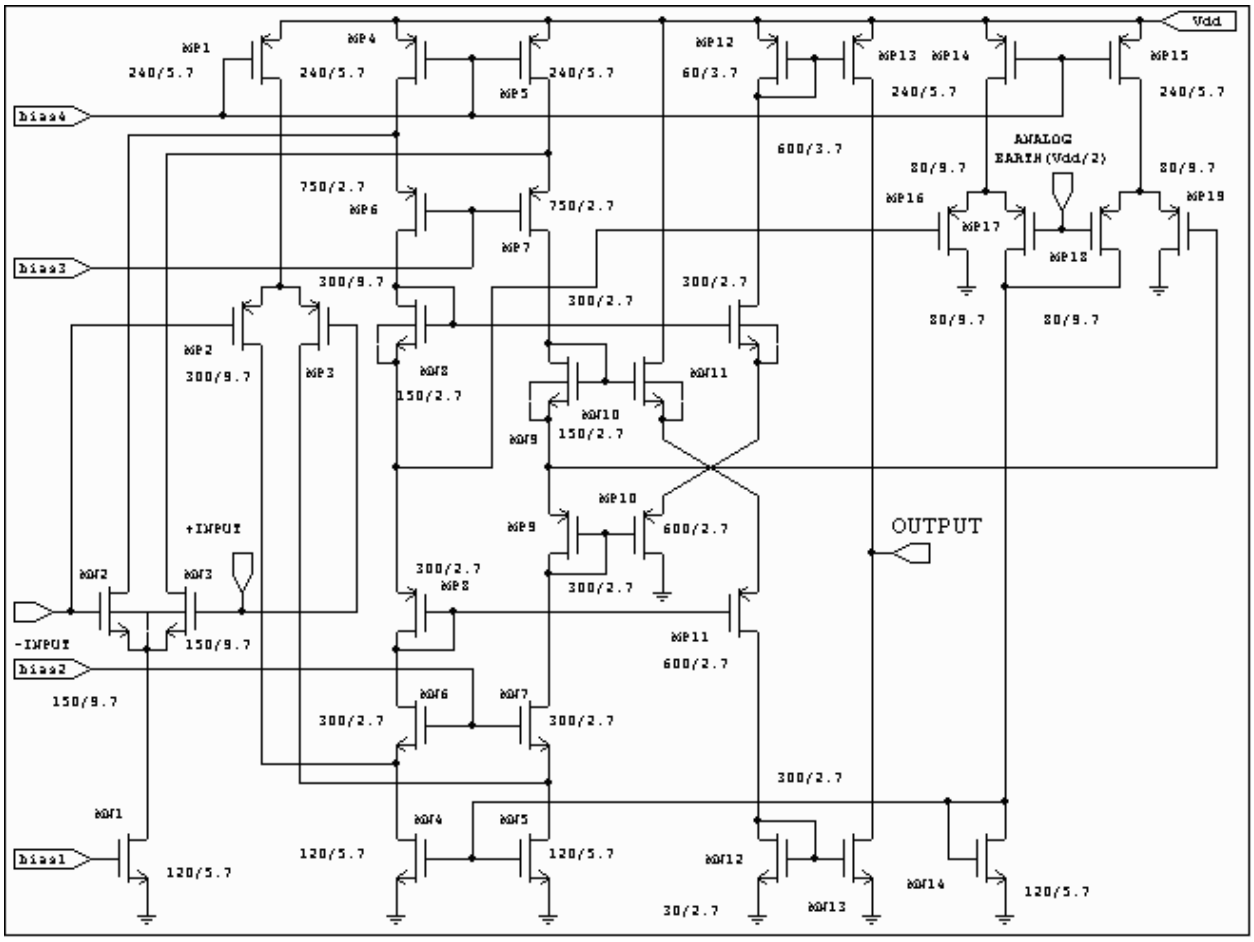


Fig. 4

4. Analog SC-macros examples

Using the analog cell library the following SC-macros has been developed: the second-order bandpass filter, the 5-th order elliptic low-pass filter and the 10-bit DAC.

The array architecture features make it desirable to use SC structures requiring the minimum number of unit capacitors for its implementation. Unfortunately, the higher SC filter pole Q-factor value is required the higher capacitance ratio should be used for SC filter designing. We have used an area-efficient SC integrator /4/ for developing the array-based second-order medium Q-factor bandpass filter. The filter circuit diagram is shown in Fig. 5, where the letter, designating appropriate capacitor, means a number of unit capacitors in this capacitor. The area-efficient integrator is used here at the first stage. The structure has a class-BP01 z-domain transfer function:

$$H(z) = \frac{(AG/BD_2)(1-z^{-1})z^{-1}}{1+(-2+\frac{AG}{BD_2}+\frac{aAE}{BD_2(D_1+a)})z^{-1}+(1-\frac{aAE}{BD_2(D_1+a)})z^{-2}}$$

Comparing with the general-form class-BP01 transfer function:

$$H(z) = \frac{Kz^{-1}(1-z^{-1})}{1+[-2+4\sin^2(\pi f_0/f_{clock})+\frac{2\sin(\pi f_0/f_{clock})}{Q}]z^{-1}+[1-\frac{2\sin(\pi f_0/f_{clock})}{Q}]z^{-2}}$$

where Q - Q-factor;

f_0/f_{clock} – pole-frequency-to-clock-frequency ratio.

and assuming:

$$A/B = C/D_2 = 2\sin(\pi f_0/f_{clock}),\ a = 1$$

it is possible to derive: Q= D2(D1+1)/E,

thus, it is significantly easier to establish a large Q-factor value due to the multiplication of D2 and D1 for the configuration considered than in the case of an ordinary filter configuration, where the Q-factor value is established by a ratio of only two capacitances.

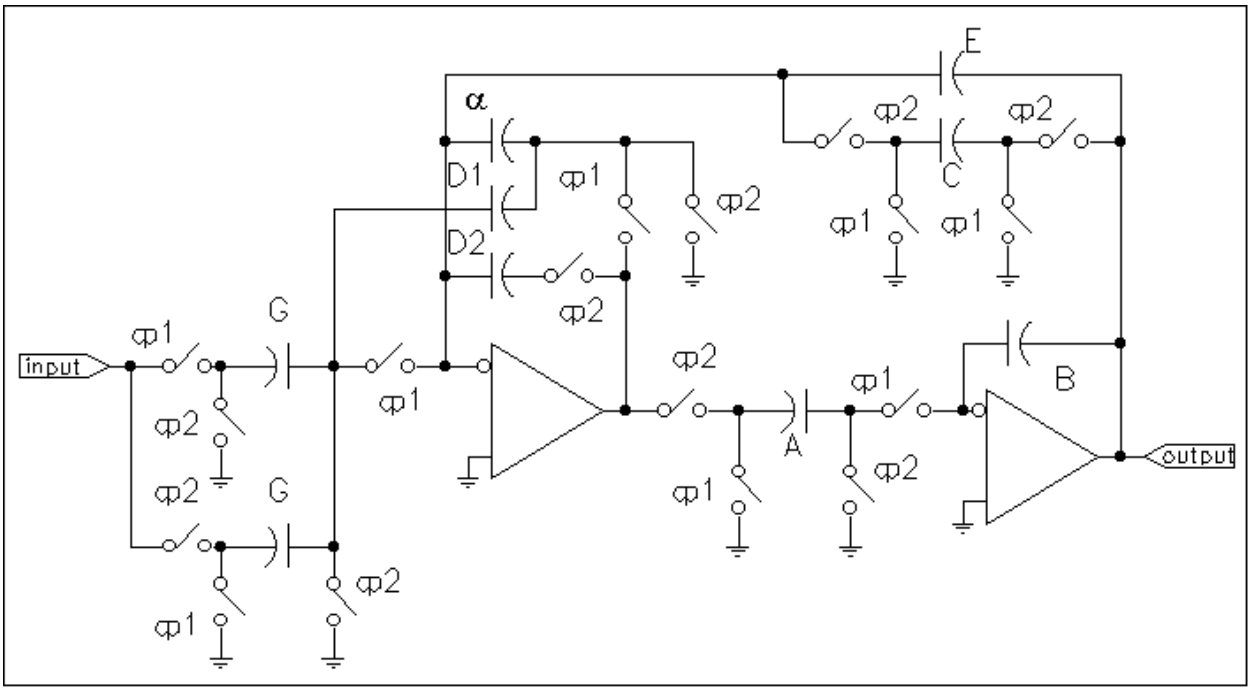


Fig. 5

The 5-th order elliptic low-pass filter is an ordinary SC ladder structure that has been developed on the basis of LC-prototype. To reduce capacitance ratios we have chosen quite a low ratio of clock frequency to filter cut-off frequency, so for correction of the discrete-time effects we developed an exact z-domain filter model. Fig. 6a shows results of SPICE simulation of the model involved and results of filter frequency response experimental measurements are shown in Fig. 6b. Unfortunately, noise floor of the testing equipment was very low - about -55 dB, so it was impossible to show the real frequency response below -55 dB level, the noise performance of the filter is, nevertheless, exellent: its dynamic range being not less than 80 dB (that was estimated "manually" by means of an oscillograph, without the automatic testing equipment); and it is impossible to detect at the filter output any clock frequency feedthrough visually by means of an oscillograph at 5 mV/div. scale, only small (about 2-3 mV) and short (few uS) output votage spikes are observed at clock frequency edges (a usual transient process, that we have seen by means of SPICE simulation too) but no output voltage modulation by the clock frequency takes place. The maximum clock frequency we have reached is about 5 Mhz and this fact is explained by the limited op amp bandwidth, nevertheless, it is not bad for the 3-um process array-based design.

For the 10-bit DAC design we have chosen a two-stage configuration employing a segmented approach similar to that proposed in /5/. The area efficiency of this configuration is much better in comparison with the classical one-stage configuration, for example, in the case of 10-bit DAC it was required about 100 unit capacitors for our DAC and for the classical one-stage configuration it is necessary to have more than 2000 unit capacitors. Of course, there are many of more area-effective DAC configurations, for example, an algorithmic DAC, but all these configurations are very slow for 10-bit resolution. The configuration considered is a sufficiently good compromise between area efficiency and speed. Moreover, the configuration considered guarantees DAC monotony even if appreciable deviations of capacitor capacities take place. To decrease the influence of op amp noise and offset voltages upon the DAC resolution the autozeroing and double-correlated sampling were introduced in the DAC configuration. The experimental measurements of the DAC show

that it ensures the 10-bit resolution.Thus, the analog-digital mixed-mode semicustom gate array-based design is proven to be a reasonable effective way of high-performance mixed-mode ASIC design using the SC technique. The grade of performance obtained through the way considered is high enough for many mixed applications and close to the full-custom design.

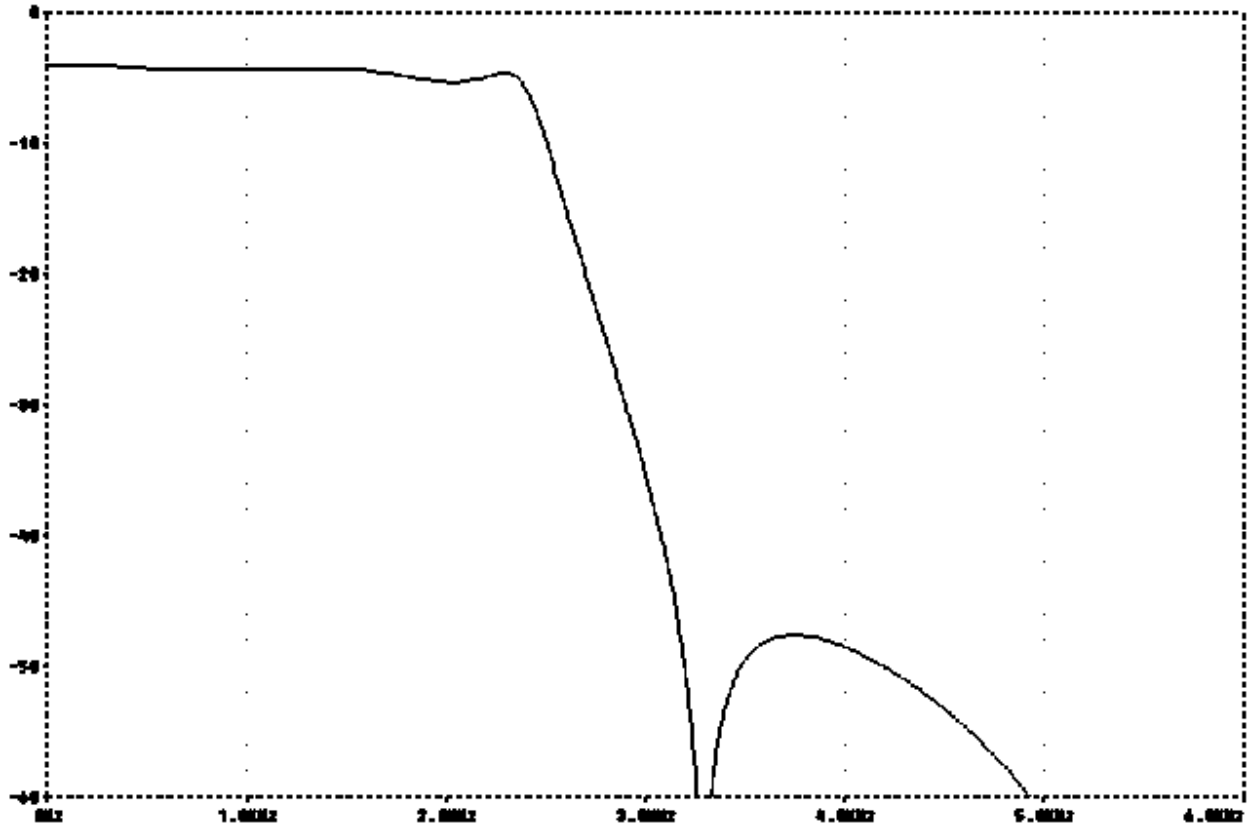


Fig. 6a

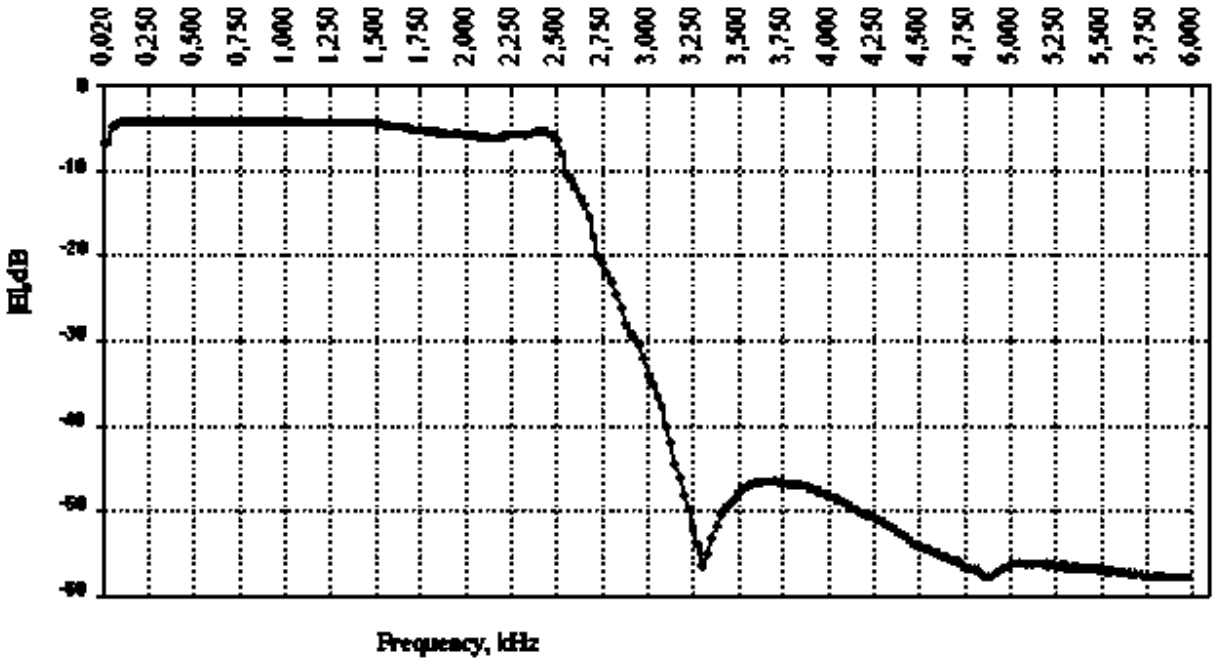


Fig. 6b

5. Summary

The switched-capacitor and switched-current techniques are known to be the basic means of analog-digital mixed-mode ASIC design. As it was shown in this paper, the semicustom-array-based SC design allows to reach close-to-full-custom performance but its main drawback is unflexibility due to the hard array architecture providing for special fixed analog fields. The functional ability (up to 42 op amps, more than 250 pF and almost 2 Mohm of overall capacitance and resistance respectively and 1500 logic gates) of the array considered, nevertheless, is high enough. To overcome the drawback involved an analog-digital symbolic design methodology is supposed to use in future work taking into account the results considered in this paper.

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