A DESIGN TECHNIQUE FOR HIGH Q-FACTOR SI FILTERS

Shlemin D.L.
Siberian State University of Telecommunications and Information Sciences.
Novosibirsk,
Russia,
e-mail

Abstract. **A problem of SI realisation of a high quality (Q) factor biquadratic filter is considered with emphasis on the signal-dependent clock feedthrough (SDCF) influence upon sensitivities of filter design parameters. The CMOS digital gate array-based implementation of medium Q-factor biquad resulted in a high random deviation of Q-factor value. An explanation of the phenomenon considered has been found by means of biquad model analysis taking into account the SDCF effect. It has been shown that a significant reduction of Q-factor sensitivities is possible to achieve through the use of an optimised DC- transfer-function voltage-to-current converter (VCC). A new S^2I memory cell utilising this VCC has been proposed and its advantage compared to the current state-of-the-art S^2I memory cell demonstrated.**

1. Introduction

The interest to analogue sampled-data switched-current (SI) systems has recently increased due to a possibility of signal processing SI system implementation using a standard CMOS VLSI digital process without any additional steps. While the SI circuit technique develops rapidly SDCF, nevertheless, remains a serious problem for SI systems. The SDCF error voltage is able to cause quite a large difference between the ideal system characteristics derived from simulation and the real ones. The problem involved becomes even more serious when a designer attempts to implement a SI system with high Q-factor pole transfer function. In this case the SDCF error voltage is able to cause system instability. Some SDCF reduction circuit techniques for SI systems are known. The most useful one is an enhanced S^2I technique /1/ that demonstrated state-of-the-art performance and is widely used for low Q-factor pole ladder filter design. Nevertheless, for high Q-factor filter realisation, the efficiency of SDCF reduction provided by this technique is not sufficient. That is why the SI technique is not used in such areas of filter applications as pilot tone detector, DTMF receiver, etc.

In this paper a study of a possibility of using the SI technique for the medium and high Q-factor applications as well as results of CMOS digital gate array-based implementation of a SI medium Q-factor biquad are presented. Moreover, a new S^2I memory cell which could be useful for high Q-factor applications is proposed and its advantage over the state-of-the-art S^2I memory cell is demonstrated.

2. SI biquad and the problem of Q-factor sensitivity

This study was initiated owing to desire to use inexpensive CMOS digital gate arrays for implementation of signal processing systems such as pilot tone detector or DTMF receiver. To reach this goal we has chosen a configuration consisting of a biquad implementing the bandpass and notch transfer functions. The notch transfer function can be derived by means of summing the input and the inverting bandpass output signals. The general form of bandpass transfer function of BP01 class, for example, is:

$$H(z)=\frac{K_0 z^{-1}(1-z^{-1})}{1+\left[-2+4\sin^2\left(\omega_0 T/2\right)+\frac{2\sin\left(\omega_0 T/2\right)}{Q}\right]z^{-1}+\left[1-\frac{2\sin\left(\omega_0 T/2\right)}{Q}\right]z^{-2}}$$

where ω_0 is the angular frequency of the transfer function pole, Q is the Q-factor , T is the clock period and K_0 is a constant.

The structure with the BP01 transfer function was synthesised and shown on Fig. 1. The transfer function of the structure considered is:

$$H(z)=\frac{I\cdot z^{-1}(1-z^{-1})}{1+(-2+E+C)z^{-1}+(1-E)z^{-2}},$$

where E, C, and I are filter coefficients.

The main advantage of this structure is that it has small filter parameter sensitivities to variations of filter coefficients' values. For example, Q-factor sensitivities are:

$$S_E^Q=-1;\quad S_C^Q=0.5.$$

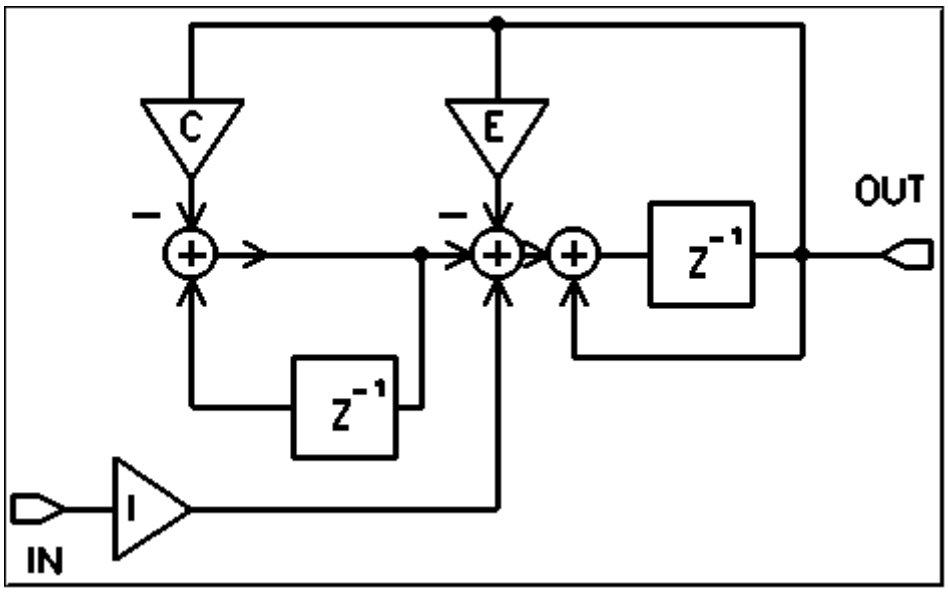


Fig. 1

For the signal processing application considered it is necessary to establish a medium Q-factor value of about 7. So, for C=0.2 chosen by us it was necessary to make the value of the E coefficient equal to 0.067.

The fully differential SI realisation of the structure considered with this set of coefficients was implemented on the base of a 3-micron CMOS digital gate array. This implementation required about 400 logic gates. The filter was designed using SI memory cells with negative feedback which were similar to fully balanced SI cells in /2/. The chip microphotograph is shown on the Fig. 2.

The experimental tests of the filter show that the random deviation of pole frequency from its nominal value was relatively small - less than 0.6 %, but the random deviation of Q-factor value was unsatisfactory large - about 25 % (nevertheless, 60 % of chip samples had less than 5 % Q-factor deviation). The ideal frequency response of the biquad considered and a set of real ones with 5 % Q-factor deviation are shown on the Fig. 3. The dynamic range of the system is better than 55 dB which is better than the digital signal processing with 8-bit resolution. It is important to note that more than 3600 CMOS logic gates are necessary for the implementation of the filter structure shown on Fig. 1 by means of 8-bit digital signal processing (not taking into account ADC and DAC). Thus, the SI technique makes it possible to decrease the chip area drastically in comparison with the digital signal processing with the same dynamic range at the expense of transfer function accuracy decrease. So, the further development of the SI technique seems very important. Since Q-factor sensitivities to coefficients variations are small for the configuration considered we suppose that the main reason of the phenomenon observed is the SDCF effect.

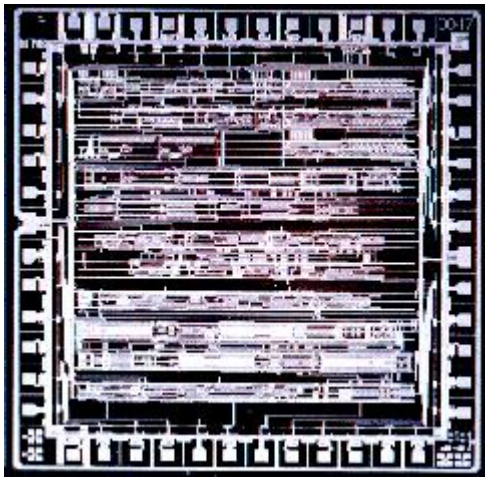


Fig. 2

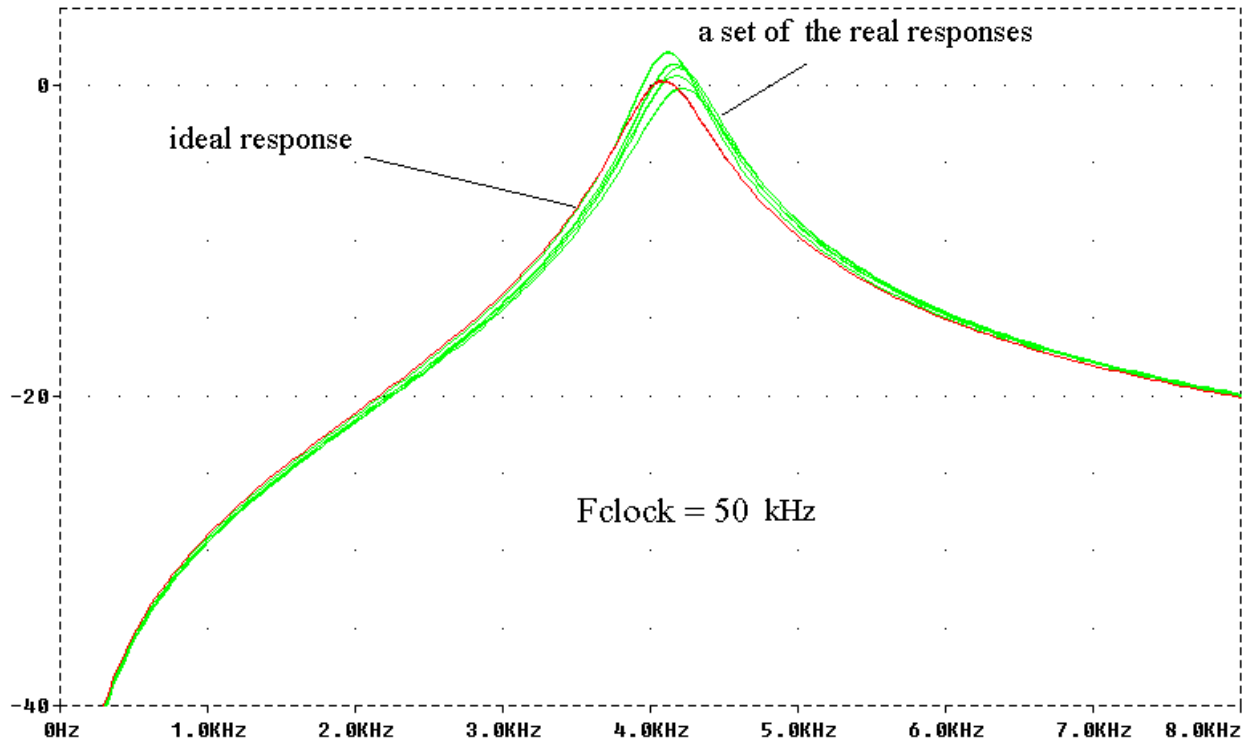

a set of the real responses
ideal response
Fclock = 50 kHz
0
-20
-40
0Hz
1.0KHz
2.0KHz
3.0KHz
4.0KHz
5.0KHz
6.0KHz
7.0KHz
8.0KHz

Fig. 3

3. Analysis of the SDCF effect in SI biquad

To prove the above supposition it is necessary to consider a SI biquad model taking into account the SDCF effect. Moreover, as the non-linear I-V and V-I conversions take place in SI circuits it is reasonable to study the influence of the function form of these conversions upon the SDCF effect. Note that the aspect mentioned was not investigated in detail yet. Some authors emphasised that the linear I-V and V-I conversions in SI circuits are better than the square root I-V and square law V-I conversions performed using saturated MOS transistors. But, as shown below, there are direct V-I and, respectively, inverse I-V conversions which are better than the linear ones in terms of reduction of SDCF effect influence.

First of all, let us consider the basic circuit of SI circuit technique - the current mode memory cell. For taking into account the SDCF only, we consider a fully differential memory cell where signal-independent clock feedthrough is completely removed. Besides, for the generality of consideration we assume that the cell consists of ideal VCCs as active elements (Fig. 4a). To take into account the SDCF effect a simple SDCF effect model of the memory cell has been developed (Fig. 4b). In this model we assume that the MOS switches do not generate any error voltage. The SDCF error is represented by a voltage source Vc , this error voltage being directly proportional to the input voltage of the memory cell as follows:

$$V_c = kv_{in} = k \cdot f^{-1}(i_{in}) \tag{3}$$

where k is a proportionality factor (k being expressed in terms of VCC input capacitance and switch capacitance) and
f^{-1} is a function inverse to the VCC DC transfer function.

In the model considered it is supposed that the switch and VCC input capacitances do not depend on a voltage applied, therefore, the k-factor is a constant.

Let us assume for simplicity that the VCC has the following general form of DC transfer function:

$$i_{out}(v_{in}) = (v_{in})^a \tag{4}$$

For example, if ***a*** = 2 we have the saturated MOS transistor (with zero threshold voltage) case, and if ***a*** = 1 the linear conversion takes place. Therefore, the memory output current distorted by the SDCF can be expressed as follows:

$$i_{out} = z^{-1/2}(1+k)^a i_{in}. \tag{5}$$

In the case of weak SDCF (i. e. k<< 1) the output current is given by:

$$i_{out} \approx z^{-1/2}(1+ka) i_{in}. \tag{6}$$

Let us consider a one clock period delay line consisting of two current copier memory cells operating during different clock frequency phases, so the delay line output current can be expressed as follows:

$$i_{out} = z^{-1}(1+ka)i_{in}. \quad (7)$$

Analysis of the biquad structure taking into account (7) and assuming the weak SDCF effect results in the following transfer function:

$$H(z) \approx \frac{I \cdot z^{-1}\left[1-(1+ka)z^{-1}\right]}{1+(-2+E_1+C_1)z^{-1}+(1-E_1)z^{-2}}. \quad (8)$$

where:

$$C_1 = (1+ka)C - kaE,$$
$$E_1 = E - 2ka + 2kaE.$$

So, the Q-factor sensitivities to k and E variations can be expressed as follows:

$$S_E^Q \approx \frac{-E}{E-2ka}; \quad S_k^Q \approx \frac{ka}{E-2ka}. \quad (9)$$

Now the reason of the large random deviation of Q-factor is clear. If a designer wants to increase the Q-factor value, he should decrease the value of E coefficient. When E will become comparable to the 2k***a*** value, both sensitivities of Q-factor tend to reach infinity. Thus, to implement a high Q-factor biquad it is necessary to reduce the last term in the denominator of the expressions of (9) as much as possible. But all the SDCF reduction techniques known are aimed at reducing the extent of SDCF effect influence expressed here through the k parameter. It should be noted that there is another opportunity to reduce the SDCF effect, namely, choose the ***a*** value less than 1, i.e., to modify the type of VCC DC transfer function. This opportunity may be used in addition to any known technique.

Choosing the ***a*** value less than 1 means that the DC transfer function has the decreasing first derivative, so with the increase of the signal value and the SDCF error voltage at the input of the output VCC too, the VCC small signal transconductance decreases and, therefore, the SDCF error output current increase is smaller compared to the case of DC transfer function with the increasing first derivative, as for the saturated MOS transistor transfer function for example.

Thus, the main idea proposed in this paper includes the use of the VCC having the decreasing-first-derivative DC transfer function for the development of SI systems, first of all, for high Q-factor filters; and the MOS transistor implementation of this VCC. It could be seen from (9), the reduction of the ***a*** value several times means an opportunity of an increase of the Q-factor the same number of times, Q-factor sensitivities and other conditions remaining the same.

Unfortunately, the exact practical implementation of the function (4) for the ***a*** value less than 1 is impossible because at Vin=0 it has the infinite value of the first derivative. So we propose to use well-known in speech coding applications the μ-law function:

$$f(x) = \frac{\ln(1+\mu x)}{\ln(1+\mu)} \quad (10)$$

where μ is a parameter (compression factor) . So the VCC DC transfer function takes the following form :

$$i_{out}(v_{in}) = I_m \frac{\ln\left(1+\mu|v_{in}|/V_m\right)}{\ln(1+\mu)} \cdot sign(v_{in}). \quad (11)$$

where Vm, Im are values limiting the input voltage and the output current swings, respectively.

Analysis of the use of the μ-law-function VCC in a SI memory cell shows that for the close-to-zero input signal it gives a SDCF error signal which is equal to the error value in the linear case, but with the increase of input signal the error signal practically remains at a constant level and does not increase. It is the latter that has a great importance for SDCF reduction because for small input signals the SDCF error signal is negligible. In the following section we examine by means of SPICE simulations the usefulness of μ-law DC transfer function VCCs for SI circuit designing.

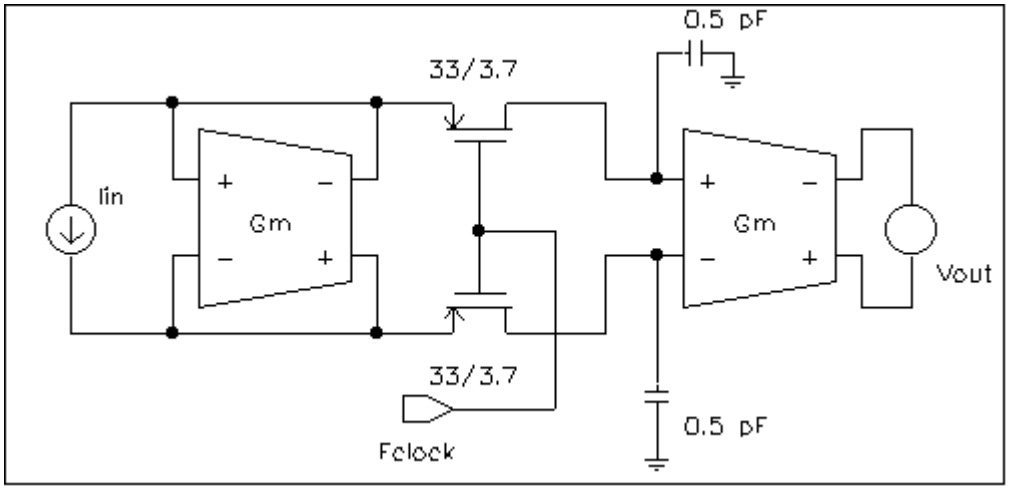


Fig 4a

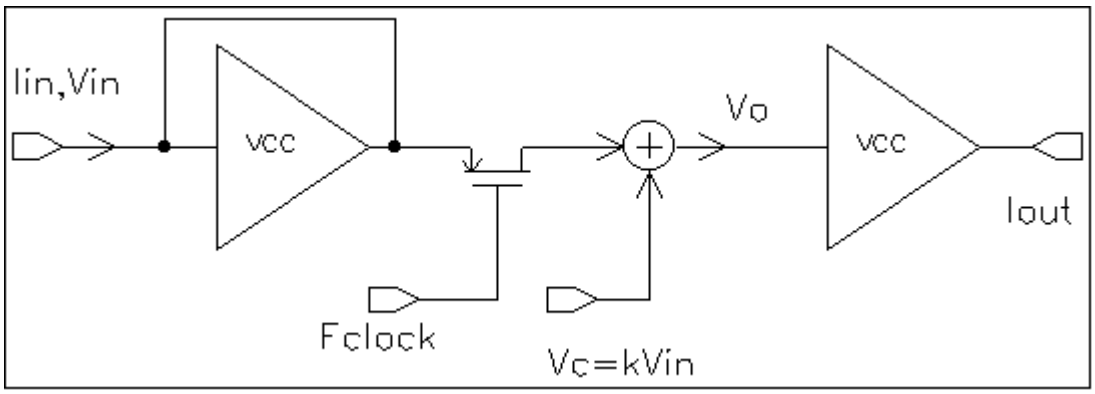


Fig4b

4. Application of the principle proposed

First of all let us consider a SI memory cell consisting of ideal VCCs for the following modifications of the VCC DC transfer functions: square-law and μ-law. Fig. 5 shows VCC transfer functions : the function (11) for three values of μ parameter (μ = 1; 10; 100) and the square law function. For all functions, Vm=1 V, Im=100 mA. It is important to note that all VCCs considered have identical input signal ranges limited by the Vm value and output current maximum values (appropriate to the Vm input voltage) limited by the Im value.

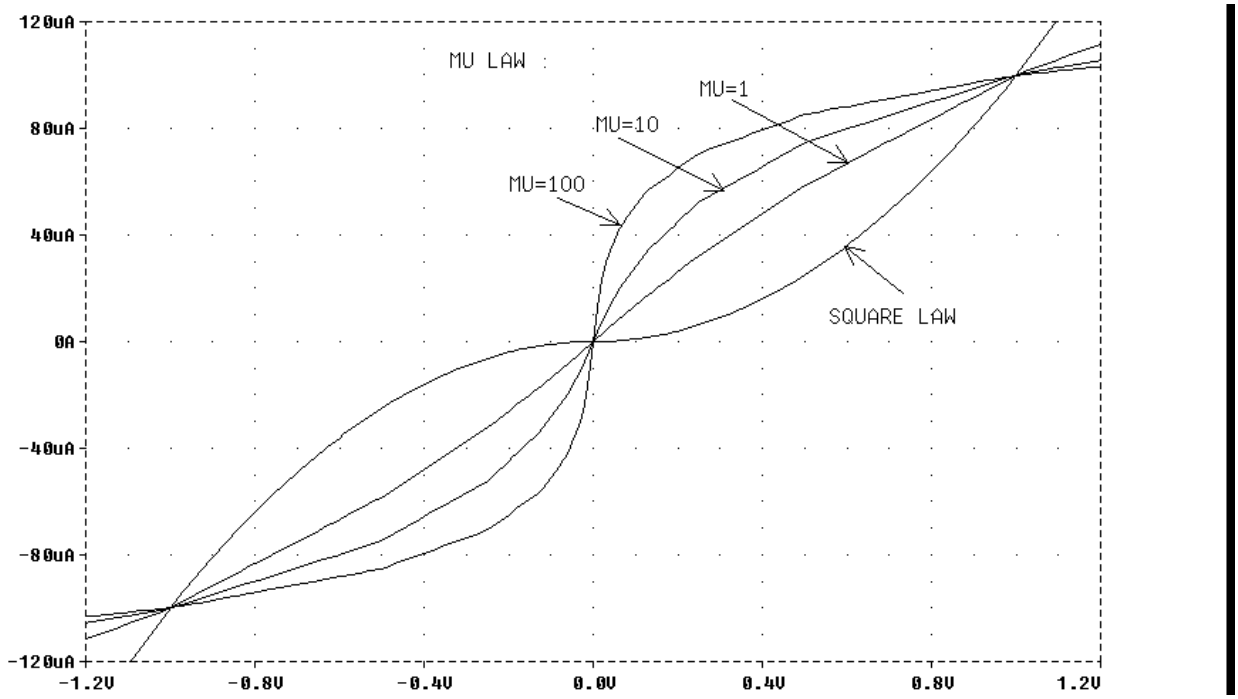


Fig. 5.

The case with μ=1 is quite close to the linear transfer function and closely corresponds to the practical realisation on the basis of a linearized MOS differential pair. The square-law case corresponds to saturated MOS transistors and the case with μ=100 is chosen to demonstrate the usefulness of the principle proposed.

Further we consider the SI memory cell shown on Fig. 4a. In this ideal memory cell the SDCF effect is taking into account by means of adding the input capacitances to the VCC inputs and using MOS transistors with appropriate parasitic capacitances as switches. Fig. 6 shows SPICE simulation results for the 100 kHz clock frequency and the 5 kHz sine wave input signal. Output signal distortions are well evident and the error signal magnitude increases sharply with the increase of input signal level.

Fig. 7 shows the effect of the use of the μ-law DC transfer function VCC: at μ=1 the SDCF distortions are less than in the square-law case but still evident; at μ=100 distortions are negligible.

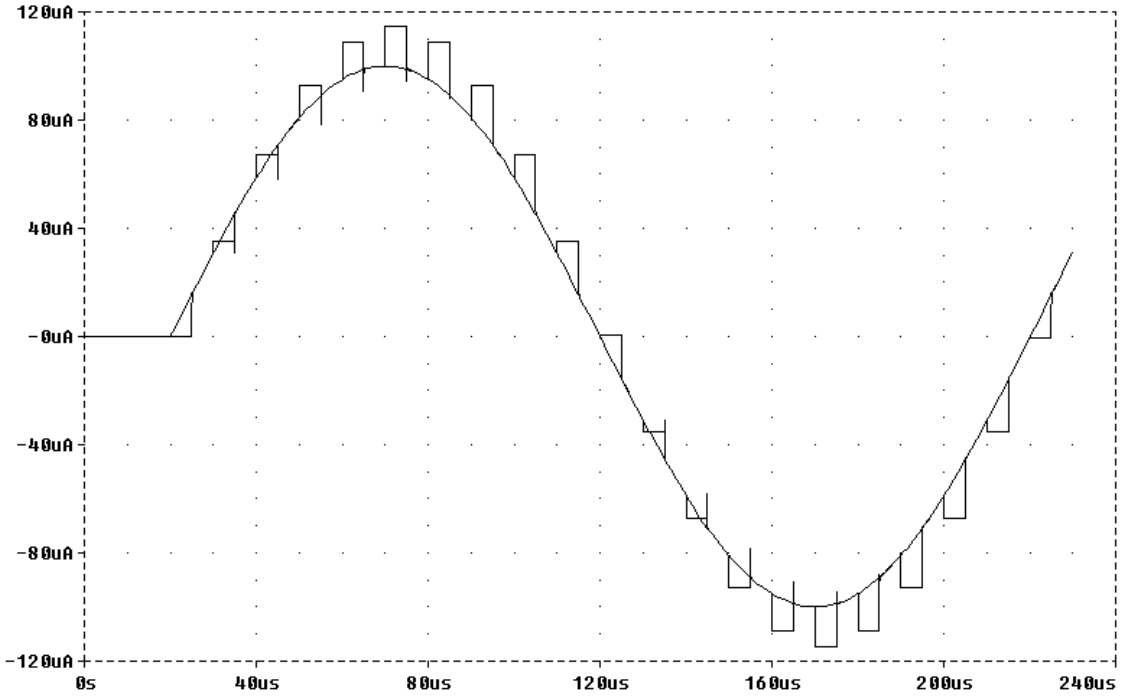


Fig. 6.

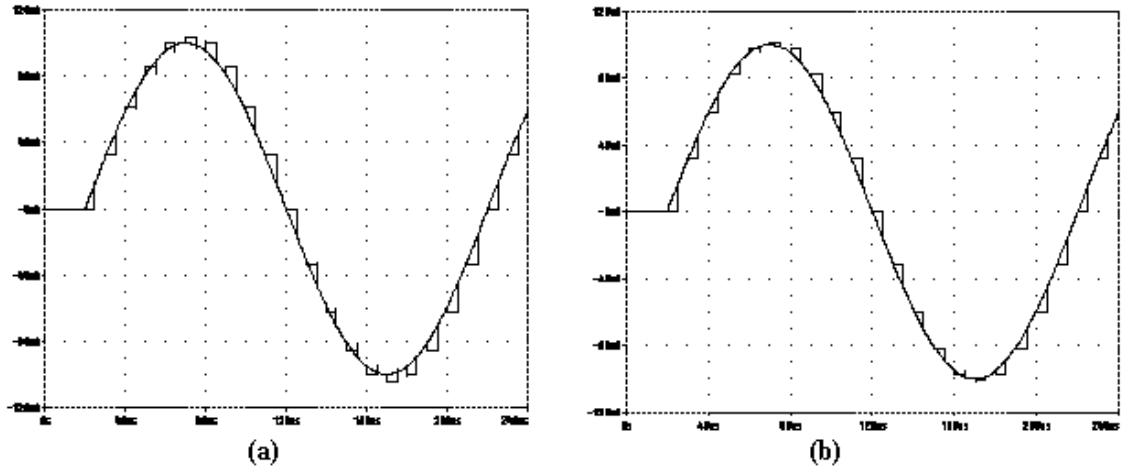


Fig.7

Fig. 7.

Now let us analytically estimate the advantage of using the VCC with μ-law DC transfer function compared to the square-law and linear ones by means of studying the SI memory cell dynamic range (DR) determined as follows:

$$(DR)^2 = s^2 / n^2 \tag{12}$$

where s^2 is the signal power, n^2 is the SDCF parasitic signal variance.

Let us assume that the memory cell input signal is a sine current:

$$i_{in} = I_m \sin(\omega_0 t)$$

It is possible to show that the upper estimate of the SDCF parasitic signal variance for the case of μ-law DC transfer function can be expressed as follows:

$$n^2 = \left[\frac{\ln(1+k)}{\ln(1+\mu)}\right]^2 I_m \tag{13}$$

Thus, the minimal advantages of the μ-law DC transfer function VCC memory cell dynamic range over the square law and linear DC transfer functions are:

$$\frac{(DR)^2_{\mu}}{(DR)^2_{sq}} = \frac{1}{2}\cdot\left[\frac{\ln(1+\mu)}{\ln(1+k)}\right]^2 (2k+k^2)^2 \tag{14}$$

$$\frac{(DR)^2_{\mu}}{(DR)^2_{lin}} = \frac{1}{2}\cdot\left[\frac{\ln(1+\mu)}{\ln(1+k)}\right]^2 k^2 \tag{15}$$

Fig. 8 shows the dynamic range advantage as a function of the k factor. It is obvious that the value of the advantage compared to the square law case can reach more than 15 dB and almost 10 dB compared to the linear one. Since the real SI system consists of quite a large number of memory cells, the total advantage can be considerable.

Now let us study the effect of μ-law DC transfer function VCC application for the SI biquad realisation by means of substituting ideal memory cells to the biquad configuration (Fig. 1) to realise the delay lines. As the small signal analysis is not valid for the SDCF effect study, let us consider the biquad impulse response and set an SDCF influence extent by means of an M factor for switch transistor size, i. e., the aspect ratio of these transistors is M and, for M=1, W/L=3/3. Thus, the M value increase is equivalent to the increase of the k-factor of our SDCF influence model. As the k-factor is process-dependent it is very desirable for the high Q-factor SI filters to have performance parameters sensitivities to the k-factor as small as possible.

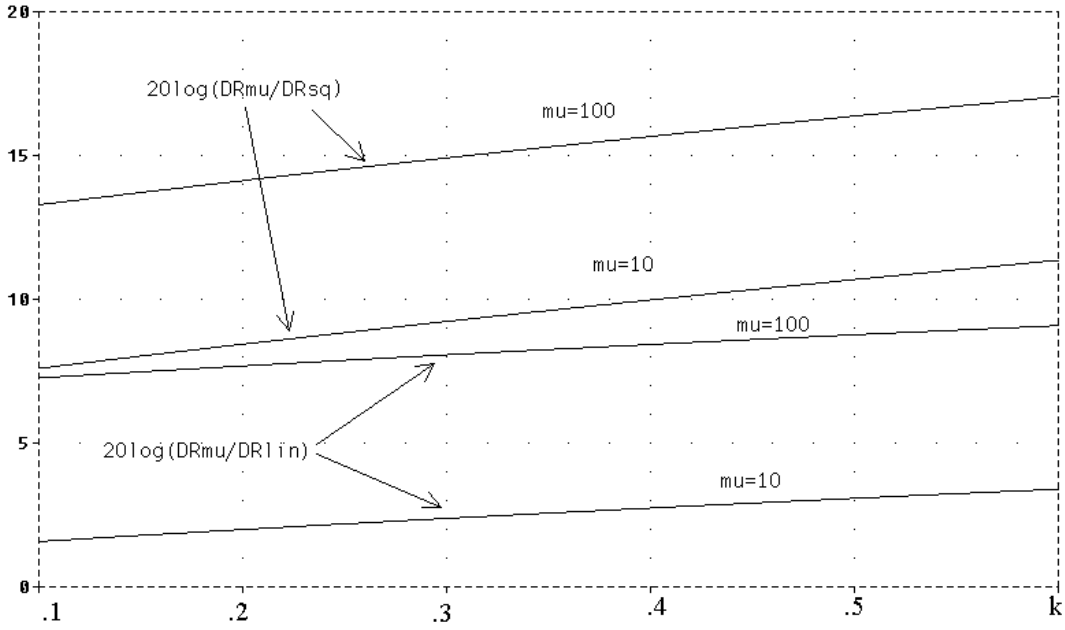
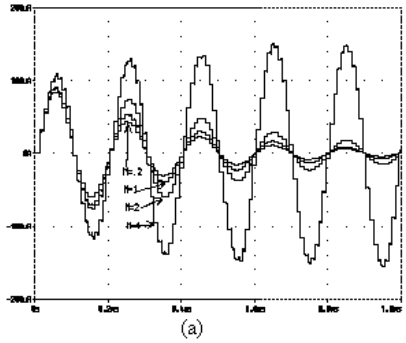
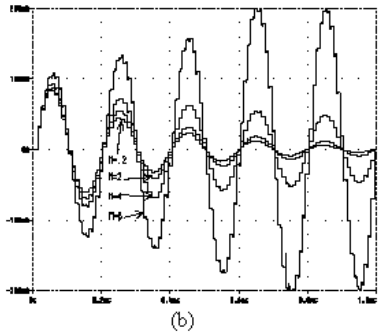


Fig.8.


(a)


(b)

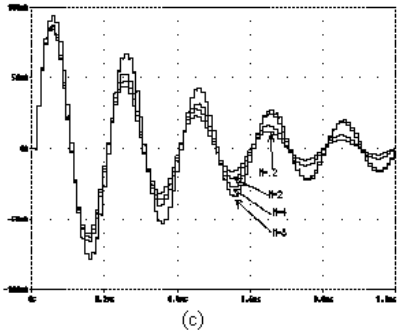

(c)

Fig. 9

Fig. 9 shows the SPICE simulation of SI biquad impulse responses for the following cases:
a) ideal square - law DC transfer function VCCs;
b) ideal linear DC transfer function VCCs;
c) ideal μ - law DC transfer function VCCs.

It is obvious from the diagrams that the filter for the square law case is unstable for M=4 and that this filter has a high Q-factor sensitivity to M variations. The filter for thelinear case is more stable but, nevertheless, it becomes unstable for M=8. The filter for the μ - law case is significantly less sensitive to M variations and stable even for M=8.

So the advantage of the technique proposed is demonstrated for a stand-alone SI memory cell and a SI biquad. The only problem to consider is the practical implementation of the VCC with the μ-law DC transfer function. We propose to use a certain number of parallel-connected MOS differential pairs. Thus, the whole DC transfer function consists of some number of segments. Each segment is represented by an appropriate differential pair. The number of differential pairs depends on the selected μ-factor value. In particular, at μ=100, it is possible to reach a satisfactory approximation degree using four MOS transistor pairs.

5. A S^2I modification of the technique proposed

As mentioned above, the proposed technique can be applied in conjunction with other well known SDCF reduction techniques. As the S^2I technique proposed in /1/ is the state-of-the-art one up to date, further we propose a S^2I memory cell version of the technique considered in this paper and show significant advantage of this cell over the enhanced S^2I memory cell (see Fig.10) proposed in /1/.

The main idea of the S^2I technique is the two-step memorising process approach: a coarse step (during the ϕ1a time slot) in which the input sample is memorised in the coarse memory (nMOS on Fig. 10) approximately followed by a fine step (during the ϕ1b time slot) in which the error of the coarse step is derived and memorised in fine memory (pMOS on Fig. 10). The output is then delivered from both memory cells so that the coarse error is subtracted to obtain an accurate copy of the input sample. So the input phase ϕ1 is subdivided into two phases: ϕ1a and ϕ1b.

The signal transmission error of a S^2I memory cell is:

$$\varepsilon_{S^2I} \approx \varepsilon_C \cdot \varepsilon_F, \qquad (16)$$

where ε_C is the coarse memory error and ε_F is the fine memory error.

Though the ε_{S^2I} value is significantly less than the signal transmission error of the ordinary SI memory cell, nevertheless, due to the use of saturated MOS transistors in the coarse memory the associated error is still unsatisfactory large for high Q-factor filter realisation. So we propose a new S^2I memory cell in which the main principle considered in this paper is applied.

In the memory cell proposed the MOS approximation of μ-law DC transfer function considered above is used only for the coarse memory realisation for the simplicity, but it is possible to use it for the fine memory realisation too which will result in further SDCF reduction.

To demonstrate the advantage of the memory cell proposed over the state-of-the-art one let us consider the results of SPICE simulation of both cells. To maintain the equal conditions in both cases we split the gates of the MOS differential pairs and switch nodes by ideal voltage followers and add capacitors to the followers' inputs. Under these conditions the SDCF error voltage amplitude is the same in both cases. Fig. 11 shows the results of SPICE simulation.

In the case of proposed memory cell the ideal output signal and the real one are very close to each other, so we show on Fig. 11 the comparison of the error signal of proposed cell with the state-of-the-art one. It is possible to see on Fig. 11 that the advantage of the cell proposed over the state-of-the-art one reaches more than the order of magnitude. It is interesting to note that in the S^2I memory cells the SDCF effect results in the decrease of the output signal while in the ordinary SI memory cells the SDCF effect increases the output signal. This phenomenon leads to the reduction of the filter's real Q-factor value compared to its ideal value but application of the proposed cell permits to minimise this reduction.

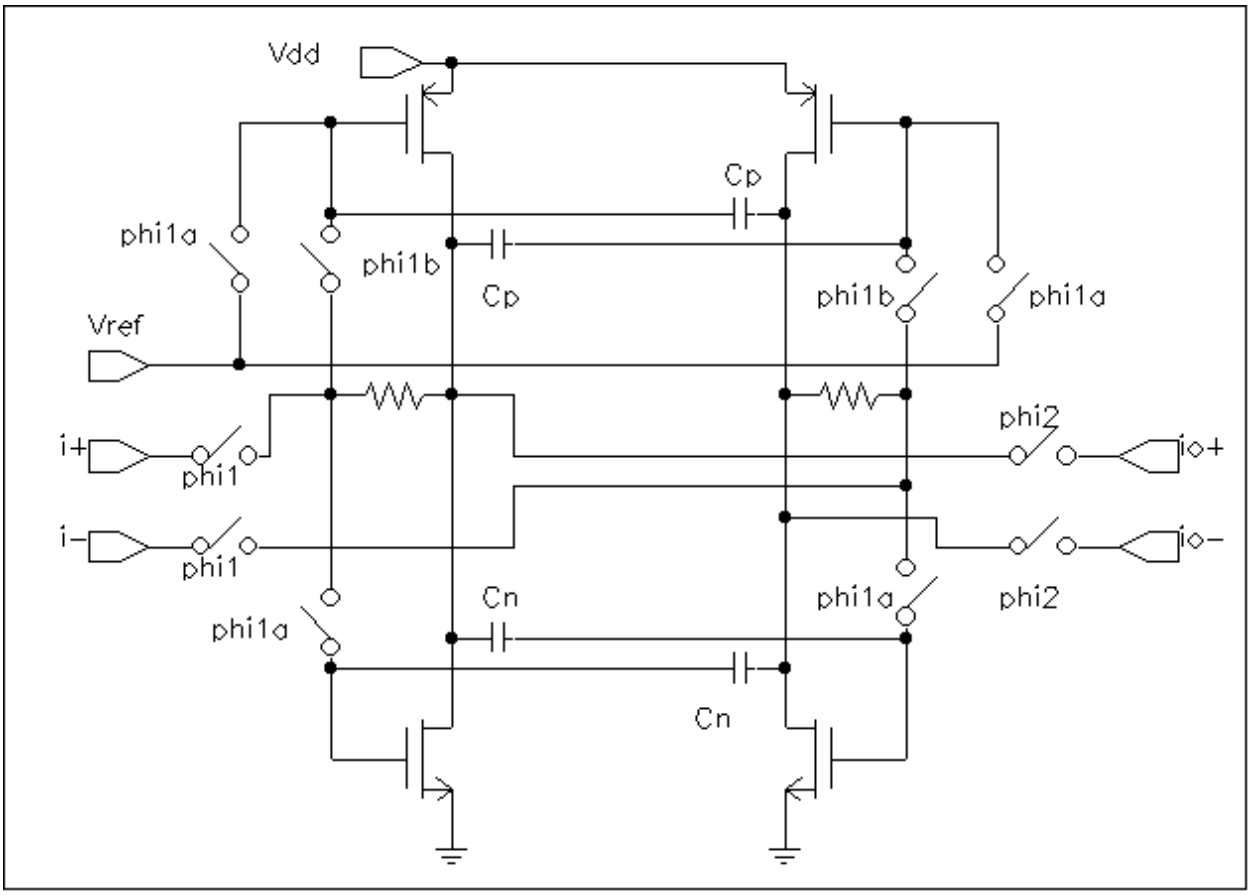
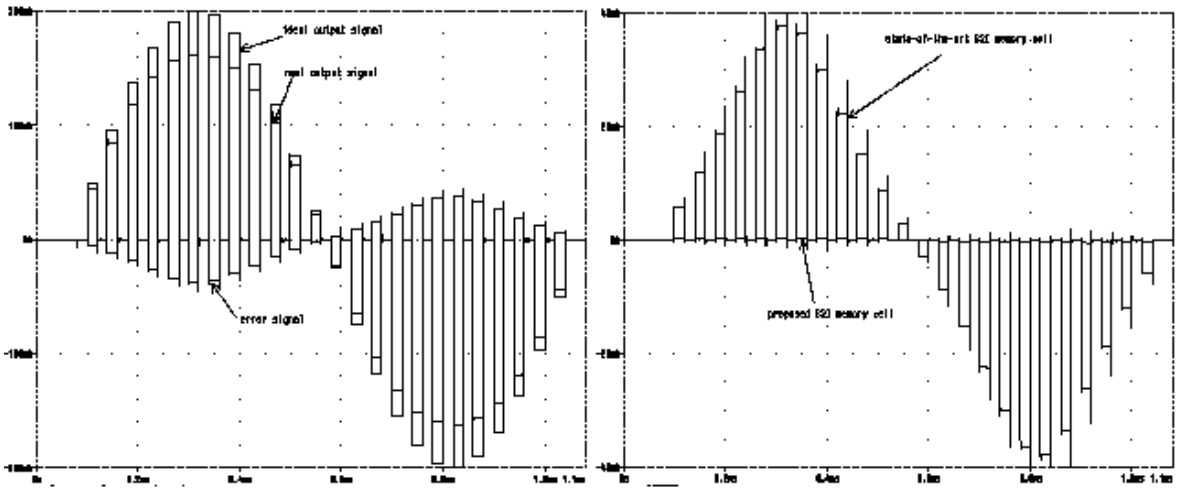


Fig. 10.



(a)

ideal output current of state-of-the-art S2I track-and-hold circuit and the real one

(b)

error signal of state-of-the-art S2I track-and-hold circuit and error signal of the proposed one

Fig.11.

Fig. 11.

6. Conclusions

In this paper the problem of high Q-factor filter SI implementation has been studied. It has been shown that the SDCF effect is the main obstacle to the goal considered. The design technique based on the use of the μ -law DC transfer function VCC has been proposed and its efficiency demonstrated by means of SPICE simulation. A new S^2I memory cell using the technique considered has been proposed. As shown by means of SPICE simulations the advantage of this cell over the state-of-the-art one reaches more than the order of magnitude in terms of SDCF distortions.

Unfortunately, up to date the author did not have any opportunity to examine the technique efficiency by means of test chip implementation and measurements but the technique usefulness is supposed to be proven by the SDCF effect model analysis and SPICE simulation results submitted in the paper.

References

1. J. B. Hughes et al.,”Automated Design of Switched-Current Filters”, IEEE J. Solid-State Circuits, vol. 31, no. 7, pp. 898-907, July 1996.

2. J. B. Hughes, K. W. Moulding, ”Switched-Current Signal Processing for Video Frequencies and Beyond”, IEEE J. Solid-State Circuits, vol. 28, no. 3, pp. 314-322, Mar. 1993.

3. T. S. Fiez, D. J. Allstot, “Switched-Current Circuit Design Issues”, IEEE J. Solid-State Circuits, vol. 26, no. 3, pp. 192-202, Mar. 1991.